REMARKS/ARGUMENTS

The foregoing amendment and the following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

35 U.S.C §112 Objections

Claims 9, 17, and 26 are rejected under 35 U.S.C. §112, first paragraph, for failing to comply with the enablement requirement. Accordingly, claims 9, 17, and 26 have been amended, support for which may be found on page 7, last paragraph, of Applicant's disclosure.

Claim 10 was rejected under 35 U.S.C §112, second paragraph, for insufficient antecedent basis for the term "the connectivity unit". Claim 10 has been amended to correct this error and is presently in condition for allowance.

35 U.S.C. §103 Rejections

Examiner rejected claims 1-16 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 5,892,962 (hereinafter "Cloutier") in view of U.S. Patent No. 5,603,043 (hereinafter "Taylor"). Particularly, the Office Action asserts that all limitations of claims 1, 10, and 18 are taught by Cloutier, except for limitations in these claims relating to a plurality of removable complex arithmetic units, which is allegedly taught by Taylor. Therefore, the Office Action concludes, it would have been obvious to one of ordinarily skill in the art to combine Cloutier and Taylor to arrive at what is claimed in claims 1, 10, and 18.

Claims 1, 10, and 18 as presently amended, include a limitation of claims 2, 11, and 19, respectively, relating to each CAE having a sequencer and an arithmetic unit. The Office Action alleges that Cloutier teaches a sequencer in element 108, column 3, lines 33-36. However, the cited reference in Cloutier in teaches a processor having a number of Field Programmable Gate Arrays (FPGA) and only one sequencer to issue control information to all of the FPGAs. In fact, nowhere in Cloutier is there taught a scaleable functional unit in a re-targetable communications processor that has a plurality of removable complex arithmetic elements, **each including a sequencer and an arithmetic unit**, as claimed in presently amended claims 1, 10, and 18.

Instead, Cloutier teaches that each of the FPGAs can be configured to perform certain operations related to image processing, pattern recognition, and neural network applications (Abstract). Taylor, in column 2, lines 5-31, describes FPGAs, how they are configured, and their disadvantages in relation to dedicated ("fully customized") logic to perform arithmetic functions, as claimed in presently amended claims 1, 10, and 18. Specifically, Taylor teaches that FPGAs must be configured by a user (Column 2, line 8) before they can perform the desired function(s). Furthermore, Taylor states that FPGAs are typically not as fast as a fully customized circuit (column 2, line 11), such as an arithmetic unit, as claimed in presently amended claims 1, 10, and 18. Furthermore, one of ordinary skill in the art will appreciate that FPGAs cannot perform the number of functions as a customized circuit, such as an arithmetic unit, without being reconfigured by a user. Therefore, Cloutier cannot be said to teach, suggest, or provide motivation for a scaleable

functional unit including a plurality of complex arithmetic elements, each having a sequencer and an arithmetic unit, as in presently amended claims 1, 10, and 18.

Somewhat similarly, Taylor teaches a system that uses an array of PLDs to perform various logical operations. However, Taylor actually teaches away from the idea that these PLDs may perform complex arithmetic functions, as the complex arithmetic elements do in claims 1, 10, and 18. For example, column 20, lines 11-15 teach that although the PLDs (included in the EPU described in the paragraph above) are useful for certain operations, arithmetic functions are better performed by logic, such as an **arithmetic logic unit**. Therefore, Taylor fails to teach, suggest, or provide motivation for a scaleable functional unit having a plurality of removable complex arithmetic elements, each having a sequencer and an arithmetic unit, as in presently amended claims 1, 10, and 18.

Neither Cloutier nor Taylor provide any teaching, suggestion, or motivation for a scaleable functional unit having a plurality of removable complex arithmetic elements, each having a sequencer and an arithmetic unit, as in presently amended claims 1, 10, and 18. In fact, Taylor actually teaches away from such a functional unit. Therefore, if the teachings of Cloutier were in fact combined with the teachings of Taylor, the two would at most teach a processing device that uses programmable logic arrays that can perform very specific, limited functions once they are programmed to do so by a user. However, the combination would not teach, suggest, or provide motivation for that which Applicant claims in presently amended claims 1, 10, and 18.

In light of the foregoing, Applicant respectfully asserts that neither claims 1, 10, 18 as presently amended, nor any claim that depends from them, can be said to

be obvious under Cloutier in view of Taylor. Accordingly, Applicant respectfully submits the present application is in condition for allowance.

If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Erik Metzger at (512) 732-3922.

If any additional fee is required, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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